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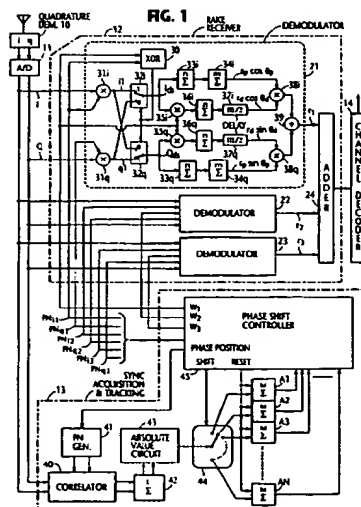
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(54) **Direct sequence spread spectrum receiver using pilot signal averaged over a fixed moving time interval.**

(57) In a direct sequence spread spectrum receiver, spread orthogonal data signals and spread orthogonal pilot signals are correlated with orthogonal despreading sequences at a chip rate. These despread signals are integrated at a symbol rate to produce orthogonal data symbols and orthogonal pilot symbols. A predetermined number of pilot symbols of each phase component is moving-averaged. Each phase component of the orthogonal data symbols is weighted with the moving average value of the corresponding phase component of the pilot symbols, and summed with the other weighted component of the data symbols to produce an output signal of the spread spectrum receiver.



The present invention relates generally to direct sequence spread spectrum (code division multiple access) receivers. This invention is particularly concerned with a direct sequence spread spectrum technique for cellular mobile communications systems in which signals are severely affected by Rayleigh fading.

Commercial interest in direct sequence spread spectrum communication systems has recently risen due to their potential ability to provide service to more users than is offered by other multiple access techniques. In the cell-site station of the DS/CDMA system, a data symbol is spread by multiplying it with higher frequency orthogonal pseudo-random number (PN) sequences assigned to the cell site as well as with orthogonal Walsh codes assigned to the channel over which the spread signal is transmitted. In order to enable the mobile station to implement synchronous acquisition and tracking operations, a pilot signal is superimposed on the data symbol sequence. At the mobile station, a sliding correlation technique is used to shift the phase timing of a local PN sequence by a predetermined amount each time a correlation is taken between the received and local sequences and determine the correct phase timing for the local sequence when the correlation exceeds some critical value. Once synchronization is established, the phase difference is monitored and maintained to within a fraction of the chip interval. During transmission, the signal undergoes reflections and scattering from various land structures, producing a complex pattern of standing waves due to mutual interference of the multipath signals at the mobile station. As a result, the propagation path of the signal exhibits a field intensity distribution which is approximated by the Rayleigh distribution. Thus, the signal experiences a phenomenon called "Rayleigh fading" and the envelope of the signal at the mobile station as well as its phase violently fluctuate.

Under such unfavorable conditions, the transmitted signal is subjected to corruption by noise and the chip-rate phase timing of the signal deviates from instant to instant from the local timing of the receiver.

It is therefore an object of the present invention to provide a direct sequence spread spectrum receiver capable of overcoming the effect of noise introduced during transmission.

According to the present invention, there is provided a direct sequence spread spectrum receiver which comprises a correlator for multiplying in-phase and quadrature spread data signals and in-phase and quadrature spread pilot signals with orthogonal despreading sequences at a chip rate to produce in-phase and quadrature despread data signals and in-phase and quadrature despread pilot signals. A data integrator provides integration of the in-phase and quadrature despread data signals at a symbol rate to produce in-phase and quadrature data symbols, and a pilot integrator integrates the in-phase and quadrature despread pilot signals at the symbol rate to produce in-phase and quadrature pilot symbols. First and second moving average circuits are provided for successively summing a predetermined number of the in-phase and quadrature pilot symbols to produce first and second moving average values, respectively. The in-phase and quadrature data symbols from the data integrator are multiplied with the first and second moving average values, respectively, by first and second multipliers. The output signal of the direct sequence spread spectrum receiver is produced by summing the outputs of the first and second multipliers. Since the pilot symbols are moving averaged and the data signals are weighted and phase rotated by the moving average values, the effect of noise on the pilot signals and consequently on the weighted and rotated data signals are reduced.

Preferably, a delay is introduced to each of the in-phase and quadrature data symbols by an amount corresponding to one half of the predetermined number of pilot symbols before being applied to the first and second multipliers. Thus, for each delayed data symbol, the moving average is derived from 1/2 of the predetermined number of pilot symbols that precede the delayed symbol as well as from 1/2 of that number that succeed it.

For multipath fading channels, it is preferable to use a plurality of demodulators and an adder connected to the outputs of the demodulators. Each of the demodulators includes a correlator for multiplying in-phase and quadrature spread data signals and in-phase and quadrature spread pilot signals with orthogonal despreading sequences at a chip rate to produce in-phase and quadrature despread data signals and in-phase and quadrature despread pilot signals. A data integrator provides integration of the in-phase and quadrature despread data signals at a symbol rate to produce in-phase and quadrature data symbols, and a pilot integrator integrates the in-phase and quadrature despread pilot signals at the symbol rate to produce in-phase and quadrature pilot symbols. First and second moving average circuits are provided for successively summing a predetermined number of the in-phase and quadrature pilot symbols to produce first and second moving average values, respectively. The in-phase and quadrature data symbols from the data integrator are multiplied with the first and second moving average values, respectively, by first and second multipliers. The output signal of the demodulator is produced by summing the outputs of the first and second multipliers and is applied to the adder.

In a further preferred embodiment, there is provided a sync acquisition and tracking circuit which includes a register for storing a plurality of phase position signals, and a first selector for cyclically selecting each one of the phase position signals in response to a shift command signal. A pseudo-random number (PN) generator produces PN sequences in accordance with the selected phase position signal and a correlator implements correlation between the in-phase and quadrature spread pilot signals and the orthogonal PN sequences to produce in-phase and quadrature despread pilot signals, which are then integrated over predetermined intervals. The integrated in-phase and quadrature signals are both squared and the results summed to produce a correlation power value. A plurality of accumulators are provided. A second selector responds to the shift command signal by cyclically selecting each of the accumulators and applying the correlation value to the selected accumulator to cause it to produce a total sum of the correlation values which are produced by the correlator during the time the phase position signal corresponding to said accumulator is repeatedly selected and applied to the PN sequence generator. The highest total sum of correlation values is selected from the outputs of all accumulators, and the phase position signal corresponding to the selected total sum is selected. The orthogonal despread sequences of the receiver are generated corresponding to the selected phase position signal. If a plurality of demodulators are used, a plurality of higher total sums are selected and corresponding phase position signals are selected to generate a plurality of orthogonal despread sequences.

The shift command signal is preferably generated at a rate much higher than the rate at which Rayleigh fading occurs.

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a direct sequence spread spectrum receiver according to the present invention;

Fig. 2 is a block diagram of the phase shift controller of the sync acquisition and tracking circuit of Fig. 1;

Fig. 3 is a graphic representation of data signals and pilot signals in a complex plane;

Figs. 4 and 5 are flowcharts describing sequences of operation performed by the controller of Fig. 2; and

Fig. 6 is a timing diagram illustrating a series of correlation values accumulated in the accumulators of Fig. 1 in relation to the signal power that varies with Rayleigh fading.

Referring now to Fig. 1, there is shown a receiving circuit of a mobile station for a DS/CDMA cellular communications system according to the present invention. At a cell-site station, a baseband downlink (cell-to-mobile) signal is initially encoded by a channel encoder into a known coded form that is optimized for radio transmission. At the chip rate much higher than the symbol rate, the symbols of the encoded signal are spread with PN (pseudo-random number) spreading sequences PN_i and PN_q commonly assigned to the service area in which the mobile station is currently located and further spread with orthogonal Walsh codes uniquely assigned to the downlink channel. A pilot signal, which may be a series of all zeros or ones, is spread at the same chip rate with the same PN sequences PN_i and PN_q with orthogonal Walsh all-zero codes. The in-phase and quadrature components of spread spectrum downlink signal are combined with the corresponding components of spread spectrum pilot signal to produce an I signal and a Q signal which are modulated onto orthogonal radio-frequency carriers, amplified and transmitted.

The spread spectrum signal from the cell-site is received by the mobile station and supplied to a quadrature demodulator 10 which includes radio-frequency amplification and demodulation stages. Using orthogonal local carriers, the demodulator 10 recovers the original in-phase signal i and quadrature signal q . Preferably, an analog-to-digital converter 11 is used to convert the i and q signals to digital form. The receiving circuit includes a RAKE receiver 12, a sync acquisition and tracking circuit 13, and a channel decoder 14.

The RAKE receiver 12 includes a plurality of identical demodulators 21, 22 and 23. For practical purposes, three demodulators are sufficient to take the multipath-fading related problem into consideration. For clarity, only demodulator 21 is shown in detail. Demodulator 21 includes a pair of multipliers 31i and 31q for multiplying the I and Q digital signals from A/D converter 11 with the pseudo-random despread sequences PN_{i1} and PN_{q1} to produce an in-phase output $i_1 = I \times PN_{i1}$ from multiplier 31i and a quadrature output signal $q_1 = Q \times PN_{q1}$ from multiplier 31q. The PN sequences PN_{i1} and PN_{q1} are the two inputs to an exclusive-OR gate 30 producing a switching signal. The output signal i_1 of multiplier 31i and the output signal q_1 of multiplier 31q are the inputs to switches 32i and 32q. If the switching signal is a binary 1, the output of multiplier 32i appears at the output of switch 32i as a signal I_{ds} . If the switching signal is a binary 0, the signal I_{ds} is equal to the output of multiplier 32q, i.e., q_1 . Similarly, the output of multiplier 31q appears at the output of switch 32q as a signal Q_{ds} when the switching signal is 1. Otherwise, the output of multiplier 31i appears as Q_{ds} . Since the pilot signal was spread at the transmitter with the all-zero Walsh code, signals I_{ds} and Q_{ds} represent the in-phase and quadrature components of the despread pilot signal.

To extract the pilot signal components, the in-phase and quadrature signals I_{ds} and Q_{ds} are respectively supplied to integrators 33i and 33q where they are integrated over the period of "n" chips (where n represents the number of chips with which the data symbol was spread at the transmitter). In order to absorb random noise, the integrators 33i and 33q are respectively followed by additional integrators, or moving average circuits 34i and 34q where the integrated I_{ds} and Q_{ds} signals are summed continuously over the period of m symbols, (where m is a predetermined number).

More specifically, each of the moving average circuits is implemented with an m-stage shift register and an adder. The shift register receives an input signal from the preceding circuit and the adder is connected to all the stages of the register for successively summing the values of their contents so that the adder produces a signal representing the moving average of the values of m pilot symbols (corresponding to m data symbols) for each phase component.

Since the data signal was spread with the channel-identifying Walsh code at the transmitter, the I_{ds} and Q_{ds} signals are applied to multipliers (correlators) 35i and 35q, respectively, where they are multiplied with a local Walsh code W_j (where $j=1$) supplied from the sync acquisition and tracking circuit 13. The outputs of multipliers 35i and 35q are fed into integrators 36i and 36q, respectively, where they are integrated over an n-chip interval to produce a replica of the original symbol for each phase component. The outputs of integrators 36i and 36q are supplied respectively to delay circuits 37i and 37q each introducing a delay of m/2 symbols. Each of the in-phase and quadrature data symbols is delayed by the interval of m/2 symbols so that the delayed symbol of each phase component corresponds to the midpoint stage of the moving average shift register. Thus, for each delayed data symbol, a moving average value is derived from m/2 pilot symbols that precede the delayed symbol as well as from m/2 pilot symbols that succeed it.

If the chip-rate timing of the PN sequences PN_{i1} , PN_{q1} and the Walsh code W_1 is in proper phase relationship with the incoming I and Q signals, the dispersed energies of the incoming signals are despread (concentrated) and the pilot signal components will appear with high amplitude at the outputs of integrators 34i and 34q as $r_p \cos \theta_p$ and $r_p \sin \theta_p$, respectively, and the data signal components will appear with high amplitude at the outputs of m/2 symbol delay circuits 37i and 37q as $r_d \cos \theta_d$ and $r_d \sin \theta_d$, respectively.

The vectors of the pilot and data signals are shown in Fig. 3. As indicated by the coordinate system of the I-Q complex plane, the amplitude of the pilot signal is usually much higher than that of the data signal and between θ_p and θ_d there is a difference $\Delta\theta$ which is negligibly small as compared with θ_p and θ_d . In order to obtain the output signal r_1 for the demodulator 21 the data signal vector is projected onto the I axis of the coordinate system by multiplying each data signal component with a complex conjugate of the corresponding pilot signal component and summing the products as follows:

$$\begin{aligned}
 r_1 &= \text{Re} [r_d \cos \theta_d (r_p \cos \theta_p - j r_p \sin \theta_p) + r_d \sin \theta_d (r_p \sin \theta_p \\
 &\quad + j r_p \cos \theta_p)] \\
 &= \text{Re} [r_p r_d (\cos \theta_p \cos \theta_d + \sin \theta_p \sin \theta_d) + j r_p r_d (\cos \theta_p \sin \theta_d \\
 &\quad - \sin \theta_p \cos \theta_d)] \\
 &= r_p r_d (\cos \theta_p \cos \theta_d + \sin \theta_p \sin \theta_d) \\
 &= r_p r_d \cos (\theta_p - \theta_d)
 \end{aligned} \tag{1}$$

Equation (1) indicates that a unit vector of the data signal is rotated clockwise to the I axis of the I-Q complex plane and weighted by the scalar product $r_p r_d$.

If several data symbols are severely corrupted by noise during transmission, the corresponding pilot symbols are moving-averaged and the effect of the noise on the pilot signal is reduced in this manner, leading to a reduction in the effect of the noise on the signal r_1 .

Returning to Fig. 1, the output signal r_1 is obtained by multiplying the in-phase pilot signal component with the in-phase data signal component by a multiplier 38i to produce an in-phase product and multiplying the quadrature pilot signal component with the quadrature data signal component by a multiplier 38q to produce a quadrature product, and summing both products by an adder 39.

In like manner, output signals r_2 and r_3 are produced by demodulators 22 and 23 and summed with the output signal r_1 of demodulator 21 by adder 24 and supplied to the channel decoder 14 where the adder output undergoes a process inverse to that of the transmitter's channel encoder.

Rotation of the data vector onto the I-axis of the I-Q complex plane allows for the simple summation of the signals r_1 , r_2 and r_3 in adder 24. The use of the pilot vector in the rotation method described above reduces the effect of fading on the signal outputted from adder 24 as the pilot vector weights the data symbol and stronger multipath signals will have stronger moving-averaged pilot strong signals which indicate low levels of fading.

Sync acquisition and tracking circuit 13 includes an orthogonal correlator 40 and a PN sequence generator 41 which generates orthogonal despreading sequences in accordance with a phase position signal from a phase shift controller 45. As will be described, the phase shift signal is generated at "window" intervals "Tw" much smaller than the intervals at which Rayleigh fading occurs. The window interval Tw is equal to $L \times T_c$, where T_c is the chip rate and L which is chosen such that during the interval of L successive chips the pilot signal never experiences more than $\pi/2$ radian rotation) PN sequence generator 41 is phase-shifted at intervals Tw and the phase shift is cyclically repeated when the PN sequence generator 41 is phase-shifted N times for each cycle (where N represents the number of phases to be shifted within interval $Tw \times N$). The I and Q data signals from A/D converter 11 are applied to the correlator 40 where the I and Q pilot signal components are despread and correlation values are detected for each pilot signal phase component during the window interval Tw. To the output of correlator 40 is connected an L-chip integrator 42 where the correlation values of each pilot signal phase component for "L" chips are summed to produce sum vectors for the in-phase and quadrature phase components of the pilot signal. The outputs of integrator 42 are fed into an absolute value circuit 43 which derives a scalar value of the resultant vector of these two vector components (i.e., the root of a sum of squares of each sum vector component) to represent the magnitude of the pilot's cross-correlation within the window interval Tw.

The output of absolute value circuit 43 is applied to an input selector 44 which is controlled by the phase shift signal to change terminal positions of its moving contact arm. Accumulators A1 to AN are connected respectively to the terminal positions of selector 43. Each of the accumulators A1 to AN provides a sum of M input signals from the corresponding terminal of selector 43 and reset in response to a signal from the phase shift controller 45. The outputs of accumulators A1 to AN are supplied to the controller 45 where they are compared with other sums to determine their ranks and select the highest three correlation values.

As shown in detail in Fig. 2, the phase shift controller 45 includes a register PRa for storing phase position signals $P1 (= \phi_0 + \Delta\phi)$ through $PN (= \phi_0 + N\Delta\phi)$ loaded from a phase position data source 51, and a register RS0 for storing correlation sum signals S1 to SN loaded from accumulators A1 to AN. Each of the phase position signals stored in register PRa is selectively supplied through a selector 52 to the PN sequence generator 41. The loading of appropriate signals into registers PRa and RS0 and the selecting of a phase position signal by selector 52 are controlled by a controller 50. Registers RS1 ~ RS3 and RP1 ~ RP3 and connected to controller 50. The highest three correlation sums are stored into registers RS1 to RS3, respectively, and corresponding phase position signals are stored into registers RP1 to RP3. The phase position signals stored in registers RP1 ~ RP3 are loaded into output registers OR1 ~ OR3, respectively, which are coupled to a Walsh code generator 53 and a PN sequence generator 54. Using the phase position signals stored in the output registers, Walsh codes W1, W2, W3, and three sets of orthogonal PN sequences PN_{i1} , PN_{q1} , PN_{i2} , PN_{q2} , PN_{i3} , PN_{q3} are generated and supplied to the demodulators 21, 22 and 23, respectively.

Initially, controller 50 commands a phase position data source 51 to load a set of phase position signals $P1 \sim PN$ into register PRa. Controller 50 includes a clock generator (not shown) and, using its clock, it generates a shift command pulse at intervals Tw and feeds it to selectors 44 and 52. The phase position signals $P1 \sim PN$ are successively selected in response to the shift command signal and applied to the PN sequence generator 41. In response to each phase position signal, the PN sequence generator 41 shifts the phase timing of despread PN sequences by $k\Delta\phi$ (where $k = 1, 2, \dots, N$). During each successive window interval Tw, L correlation values are summed by integrator 42 and applied through selector 44 to one of the accumulators A1 to AN which corresponds to the phase position signal applied during that window interval to the PN sequence generator 41. The process is repeated M times for each phase position signal and hence for each accumulator so that in the accumulator a total sum of M correlation values is stored for the corresponding phase position. When the shift command signal is generated repeatedly $N \times M$ times, the phase position signals are transferred from register PRa to a register PRb to allow a new set of phase position signals to be loaded into register PRa, while allowing the transferred phase position signals to be used during a subsequent process for the determination of higher correlation sums. At the same time, the correlation sums in the accumulators A1 ~ AN are loaded into register RS0 for making comparisons with each other to select the first, second and third largest values of correlation sums and loading corresponding phase position signals from register PRb into output registers OR1 ~ OR3.

The operation of the controller 50 will be fully described using the flowcharts of Figs. 4 and 5. In Fig. 4, sync acquisition starts with step 60 to reset all accumulators A1 to AN and load a set of N new phase position signals P1 ~ PN into register PRa from data source 51. Exit then is to step 61 to initialize a count variable h to zero. Control proceeds to step 62 to supply a shift command pulse to selectors 44 and 52, so that phase position signal P1 is initially supplied to PN generator 41, and over L times correlation values are generated by correlator 40, summed by integrator 42 and stored in accumulator A1. At step 63, count variable h is incremented by one and a check is made at step 64 to see if h is equal to or greater than N x M. If not, control returns to step 62 to read phase position signal P2 from register PRa into PN generator 41 and controller 50, and a sum of resultant L correlation values is stored in accumulator A2. Similar operations proceed until the decision at step 64 becomes affirmative, whereupon totals of correlation sums S1 through SN are stored in accumulators A1 ~ AN for phase position signals P1 ~ PN. Control proceeds to step 65 to transfer the phase position signals from register PRa to register PRb, and returns to step 60 to repeat the shift operation for a set of new phase positions.

In Fig. 5, a read operation starts at step 70 when h is equal to N x M by loading correlation sums S1 ~ SN from accumulators A1 ~ AN into register RS0 and resetting registers RS1, RS2 and RS3 to zero. At step 71, count variables i and j are reset to zero and successively incremented by one at steps 72 and 73. Count variable i (where i = 1 to 3) identifies the registers RP1 ~ RP3 and RS1 ~ RS3 and variable j (where j = 1 to N) identifies the phase position signal P1 ~ PN and the correlation sums S1 ~ SN. At decision step 74, the correlation sum Sj in register RS0 is compared to a correlation sum Si previously stored in register RSi. If Sj is larger than Si, control branches at step 74 to step 75 to set correlation sum Sj into register RSi, and locate the corresponding phase position signal Pj in register PRb and set it into register RPi. If Sj is smaller than Si, control branches to step 76 to check to see if j is equal to N. If j is not equal to N, steps 73, 74 and 75 are repeated to test for the relative value of the next correlation sum Sj with Si. Thus, S1 is initially determined to be larger than the previous value since the latter is zero and stored into register RS1 as data Si and the next correlation sum S2 is compared with S1. If S2 < S1, steps 73 to 74 are repeated, and if S2 > S1, S1 is replaced in register RS1 with S2 at step 75.

When a maximum correlation sum is determined for a set of N correlation value, the decision at step 76 becomes affirmative, and control exits the loop and enters decision step 77 to check to see if i = 3. If not, control proceeds to step 78 to remove the maximum value of register RSi from the register RS0, and control returns to step 72 to repeat the process until a third highest value is determined and stored in register RS3. When this occurs, the decision at step 77 becomes affirmative, and control advances to step 79 to load the phase position signals from registers RP1 ~ RP3 into output registers OR1 ~ OR3.

In this way, three correlation sums from the highest value are determined for a set of N correlation sums and corresponding phase position signals are stored in output registers OR1, OR2 and OR3. During the read operation, the shift operation is in progress for the next set of correlation sums for the next phase position signals.

Since the window interval Tw is much smaller than any of the intervals at which Rayleigh fading occurs and correlations are taken from sample points distributed at intervals Tw x N as illustrated in Fig. 6, Rayleigh-fading related signal power variations are also distributed and averaged out for each correlation sum. Whereas, the prior art sync acquisition and tracking circuit using a sliding window correlator has a longer window interval for correlation sums A1, A2 and A3 as indicated by dotted lines. As a result, each correlation sum of the prior art is severely affected by Rayleigh fading.

The integer M is chosen so that the product L x M, which gives an amount of chips that can be used to correct samples from the pilot signal, is sufficient to provide a valid correlation sum for each phase position, and the interval L x M x N within which N correlation sums are produced, is chosen at a value which does not exceeds beyond the tolerance of maximum frequency shift.

Claims

1. A direct sequence spread spectrum receiver comprising:
 - correlator means (30-32, 35) for multiplying in-phase and quadrature spread data signals and in-phase and quadrature spread pilot signals with orthogonal despread sequences at a chip rate to produce in-phase and quadrature orthogonal despread data signals and in-phase and quadrature despread pilot signals;
 - data integrator means (33i, 33q) for integrating the in-phase and quadrature despread data signals at a symbol rate to produce in-phase and quadrature data symbols;
 - pilot integrator means (36i, 36q) for integrating the in-phase and quadrature despread pilot signals at said symbol rate to produce in-phase and quadrature pilot symbols;

first and second moving average means (34i, 34q) for successively summing a predetermined number of the in-phase and quadrature pilot symbols to produce first and second moving average values, respectively;

first and second multiplier means (38i, 38q) for multiplying the in-phase and quadrature data symbols of the data integrator means with the first and second moving average values, respectively; and

means (39) for summing output signals of the first and second multiplier means.

2. A direct sequence spread spectrum receiver as claimed in claim 1, further comprising:

first delay means (37i) for introducing a delay to the in-phase data symbol of said data integrator by an amount corresponding to one half of said predetermined number of in-phase pilot symbols and applying the delayed symbol to said first multiplier means (38i); and

second delay means (37q) for introducing a delay to the quadrature data symbol of said data integrator by an amount corresponding to one half of said predetermined number of quadrature pilot symbols and applying the delayed symbol to said second multiplier means (38q).

3. A direct sequence spread spectrum receiver as claimed in claim 1 or 2, further comprising a sync acquisition and tracking circuit comprising:

register means (PRa) for storing a plurality of phase position signals;

first selector means (52) for cyclically selecting each one of said phase position signals in response to a shift command signal;

pseudo-random number (PN) generator (41) for producing orthogonal PN sequences in accordance with the selected phase position signal;

correlator means (40, 42, 43) for multiplying the in-phase and quadrature spread pilot signals with the PN sequences of the PN generator (41) at said chip rate to produce in-phase and quadrature despread pilot signals and integrating the in-phase and quadrature despread pilot signals at predetermined intervals to produce a correlation value;

a plurality of accumulator means (A1~AN);

second selector means (44) for cyclically selecting each one of said accumulator means in response to said shift command signal and applying the correlation value to the selected accumulator means to thereby cause same to produce a total sum of the correlation values which are produced by said correlator means while said phase position signals are being cyclically selected and applied to said PN sequence generator; and

control means (45) connected to said accumulator means (A1~AN) for generating said shift command signal at a predetermined rate, selecting a total sum of the highest correlation value from the total sums of all of said accumulator means, selecting the phase position signal which corresponds to the selected total sum, generating orthogonal desreading sequences corresponding to the selected phase position signal, and applying the orthogonal desreading sequences to said correlator means (31-32, 35).

4. A direct sequence spread spectrum receiver as claimed in claim 3, further comprising means (51) for storing therein a plurality of different sets of phase position signals and loading each one of said sets of phase position signals therefrom into said register means (RPa) when all of said accumulator means produce said total sums of correlation values for a set of phase position signals currently stored in said register means.

5. A direct sequence spread spectrum receiver as claimed in claim 3 or 4, wherein said predetermined rate at which said shift command signal is generated is higher than a rate at which Rayleigh fading occurs.

6. A direct sequence spread spectrum receiver as claimed in claim 5, wherein said predetermined rate corresponds to an interval not exceeding $\pi/2$ radian rotation of said in-phase and quadrature pilot signals.

7. A direct sequence spread spectrum receiver comprising:
a plurality of demodulators (21, 22, 23); and
an adder (24) connected to outputs of said demodulators,
each of said demodulators comprising:

correlator means (31-32, 35) for multiplying in-phase and quadrature spread data signals and in-phase and quadrature spread pilot signals with orthogonal despreading sequences at a chip rate to produce in-phase and quadrature despread data signals and in-phase and quadrature despread pilot signals;

data integrator means (33i, 33q) for integrating the in-phase and quadrature despread data signals at a symbol rate to produce in-phase and quadrature data symbols;

pilot integrator means (36i, 36q) for integrating the in-phase and quadrature despread pilot signals at said symbol rate to produce in-phase and quadrature pilot symbols;

first and second moving average means (34i, 34q) for successively summing a predetermined number of the in-phase and quadrature pilot symbols to produce first and second moving average values, respectively;

first and second multiplier means (38i, 38q) for multiplying the in-phase and quadrature data symbols of the data integrator means with the first and second moving average values, respectively; and

means (39) for summing output signals of the first and second multiplier means to produce a sum signal and supplying the sum signal to said adder (24).

8. A direct sequence spread spectrum receiver as claimed in claim 7, further comprising:

first delay means (37i) for introducing a delay to the in-phase data symbol of said data integrator by an amount corresponding to one half of said predetermined number of in-phase pilot symbols and applying the delayed symbol to said first multiplier means (38i); and

second delay means (37q) for introducing a delay to the quadrature data symbol of said data integrator by an amount corresponding to one half of said predetermined number of quadrature pilot symbols and applying the delayed symbol to said second multiplier means (38q).

9. A direct sequence spread spectrum receiver as claimed in claim 7 or 8, further comprising a sync acquisition and tracking circuit comprising:

register means (PRa) for storing a plurality of phase position signals;

first selector means (52) for cyclically selecting each one of said phase position signals in response to a shift command signal;

pseudo-random number (PN) generator (41) for producing orthogonal PN sequences in accordance with the selected phase position signal;

correlator means (40, 42, 43) for multiplying the in-phase and quadrature spread pilot signals with the orthogonal PN sequences of the PN generator (41) at said chip rate to produce in-phase and quadrature despread pilot signals and integrating the in-phase and quadrature despread pilot signals at predetermined intervals to produce a correlation value;

a plurality of accumulator means (A1~AN);

second selector means (44) for cyclically selecting each one of said accumulator means in response to said shift command signal and applying the correlation value to the selected accumulator means to thereby cause same to produce a total sum of the correlation values which are produced by said correlator means while said phase position signals are being cyclically selected and applied to said PN sequence generator; and

control means (45) connected to said accumulator means (A1~AN) for generating said shift command signal at a predetermined rate, selecting total sums of higher correlation values from the total sums of all of said accumulator means, selecting ones of said phase position signals which correspond to the selected total sums, generating a plurality of orthogonal despreading sequences corresponding to the selected phase position signals, and applying the plurality of orthogonal despreading sequences to said demodulators (21, 22, 23), respectively.

10. A receiver as claimed in claim 7, 8 or 9, further comprising means (51) for storing therein a plurality of different sets of phase position signals and loading each one of said sets of phase position signals therefrom into said register means (RPa) when all of said accumulator means produce said total sums of correlation values for a set of phase position signals currently stored in said register means.

11. A receiver as claimed in any one of claims 7 to 10, wherein said predetermined rate at which said shift command signal is generated is higher than a rate at which Rayleigh fading occurs.

12. A direct sequence spread spectrum receiver as claimed in claim 11, wherein said predetermined rate corresponds to an interval not exceeding $\pi/2$ radian rotation of said in-phase and quadrature pilot signals.

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FIG. 1

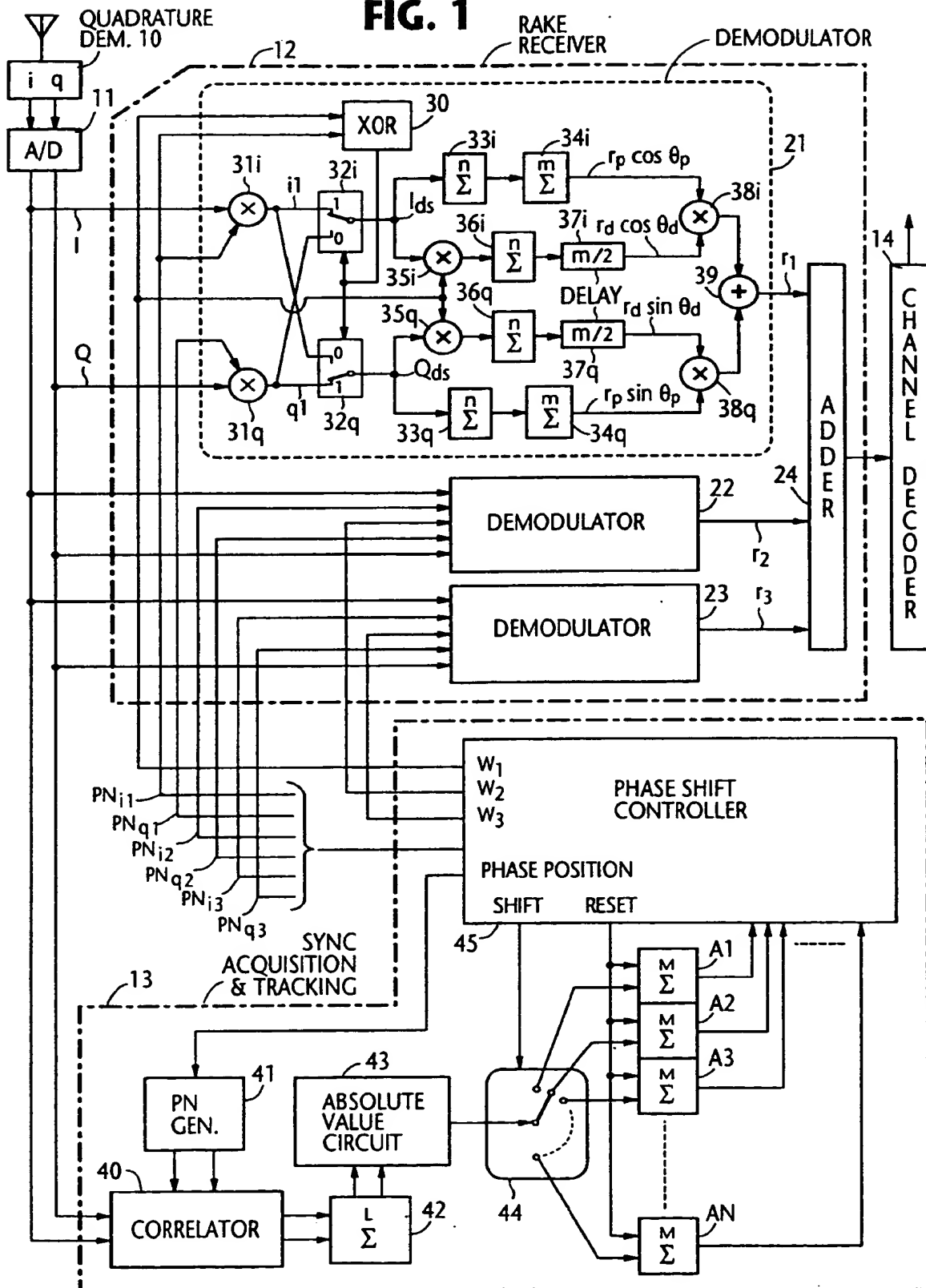


FIG. 2

PHASE SHIFT CONTROLLER 45

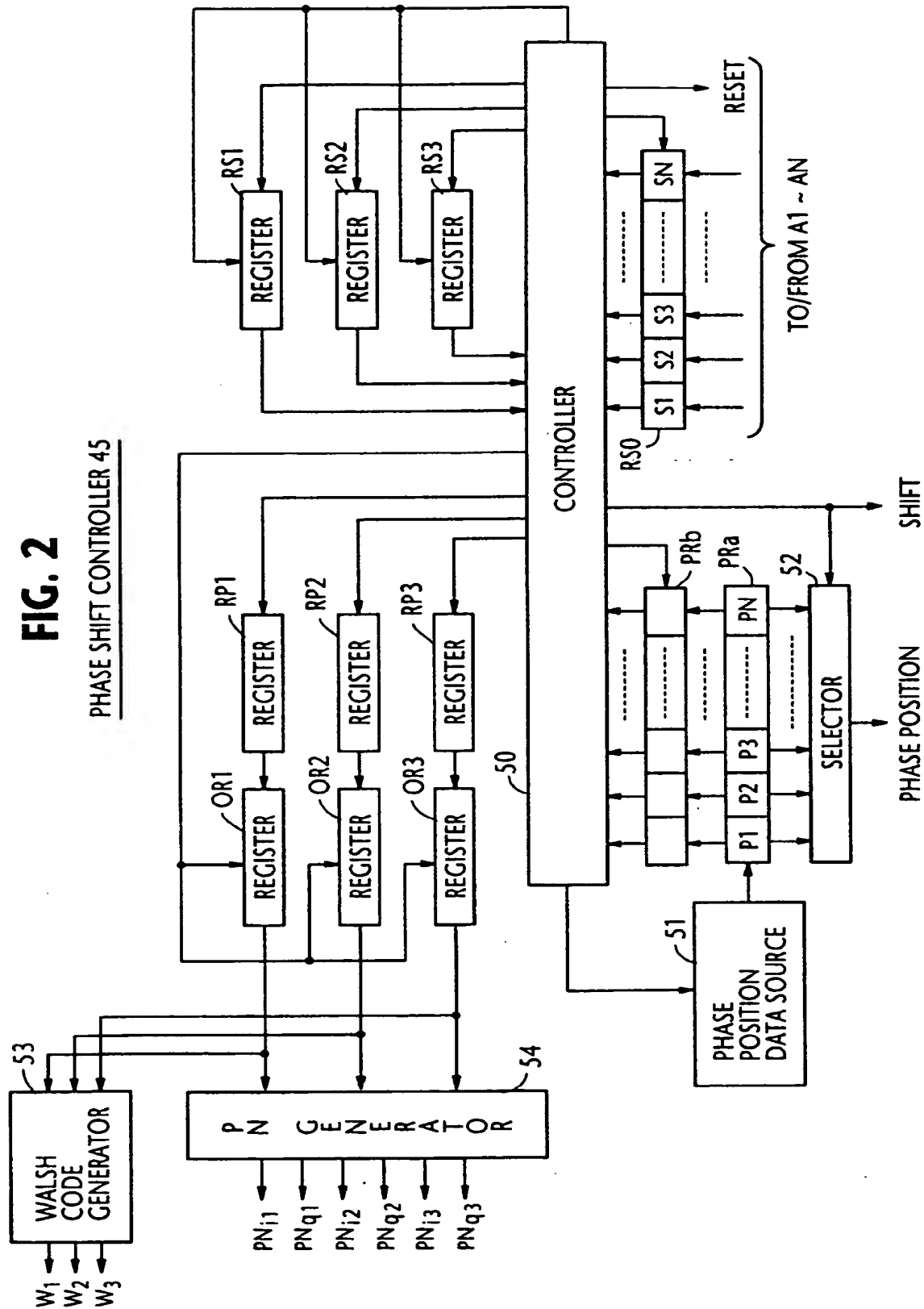


FIG. 3

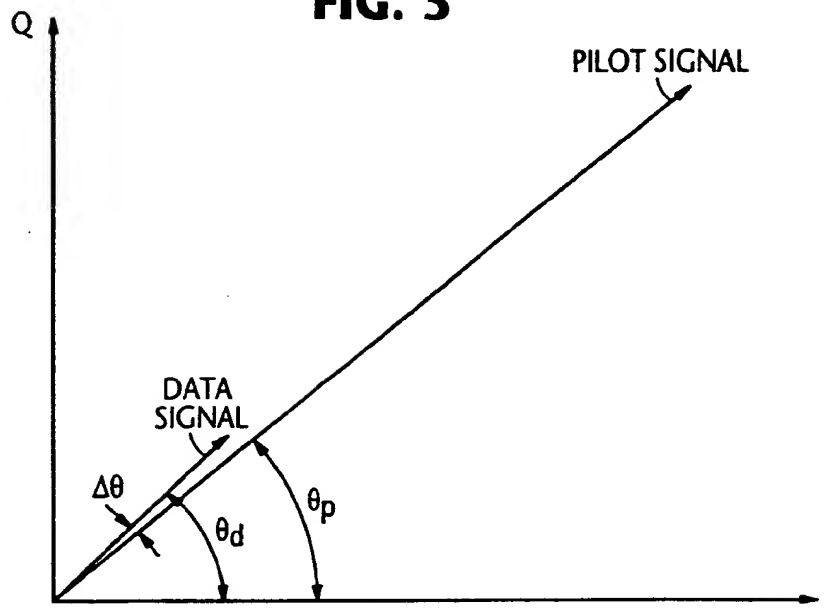


FIG. 6

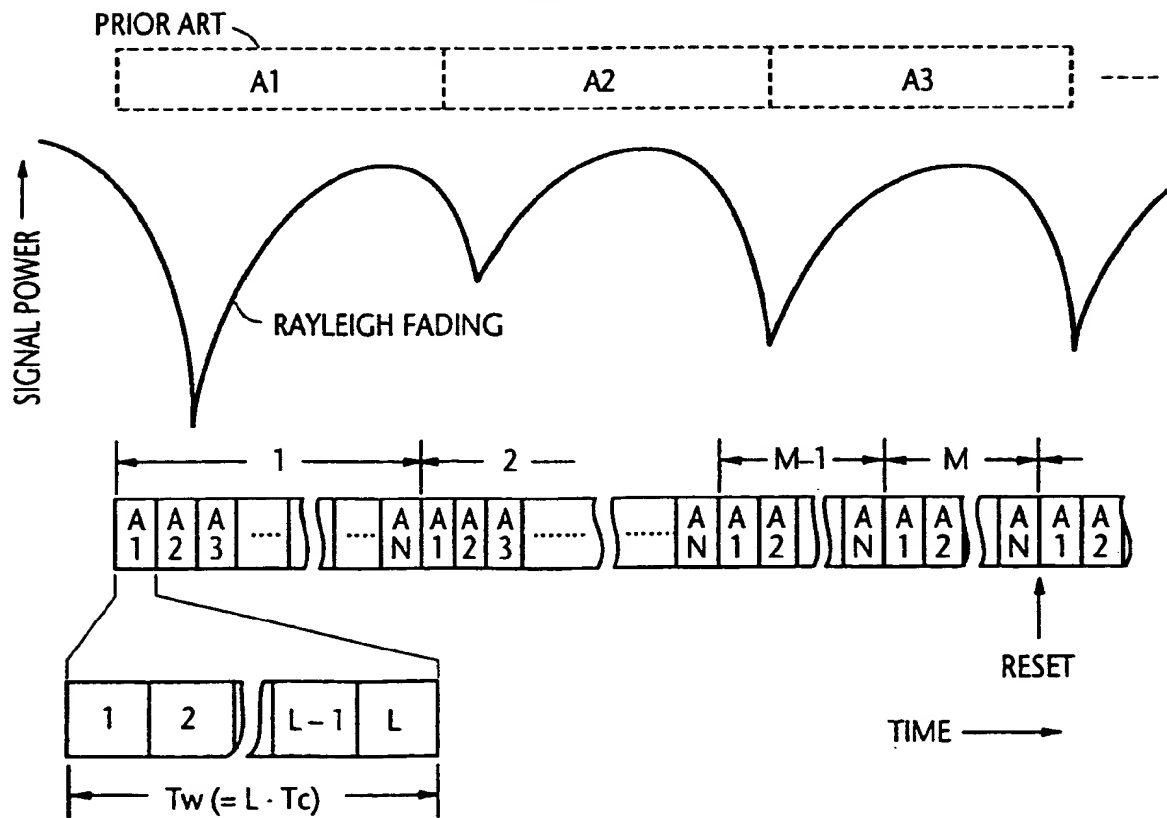
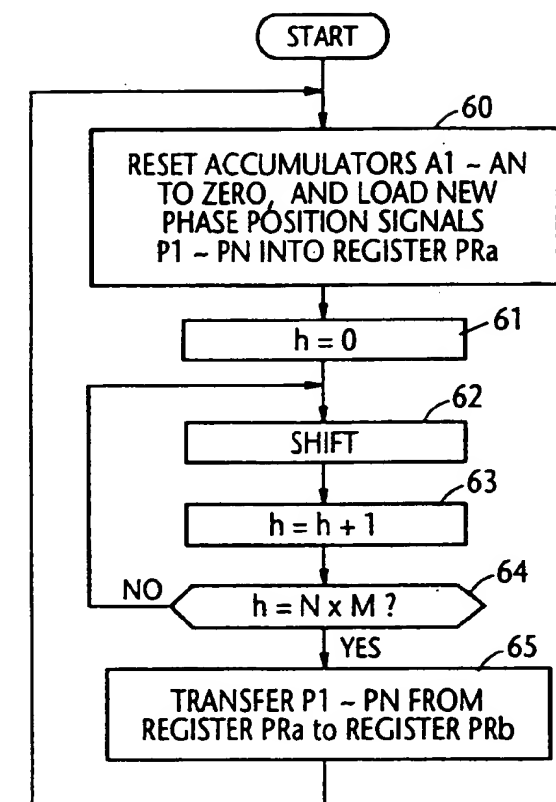
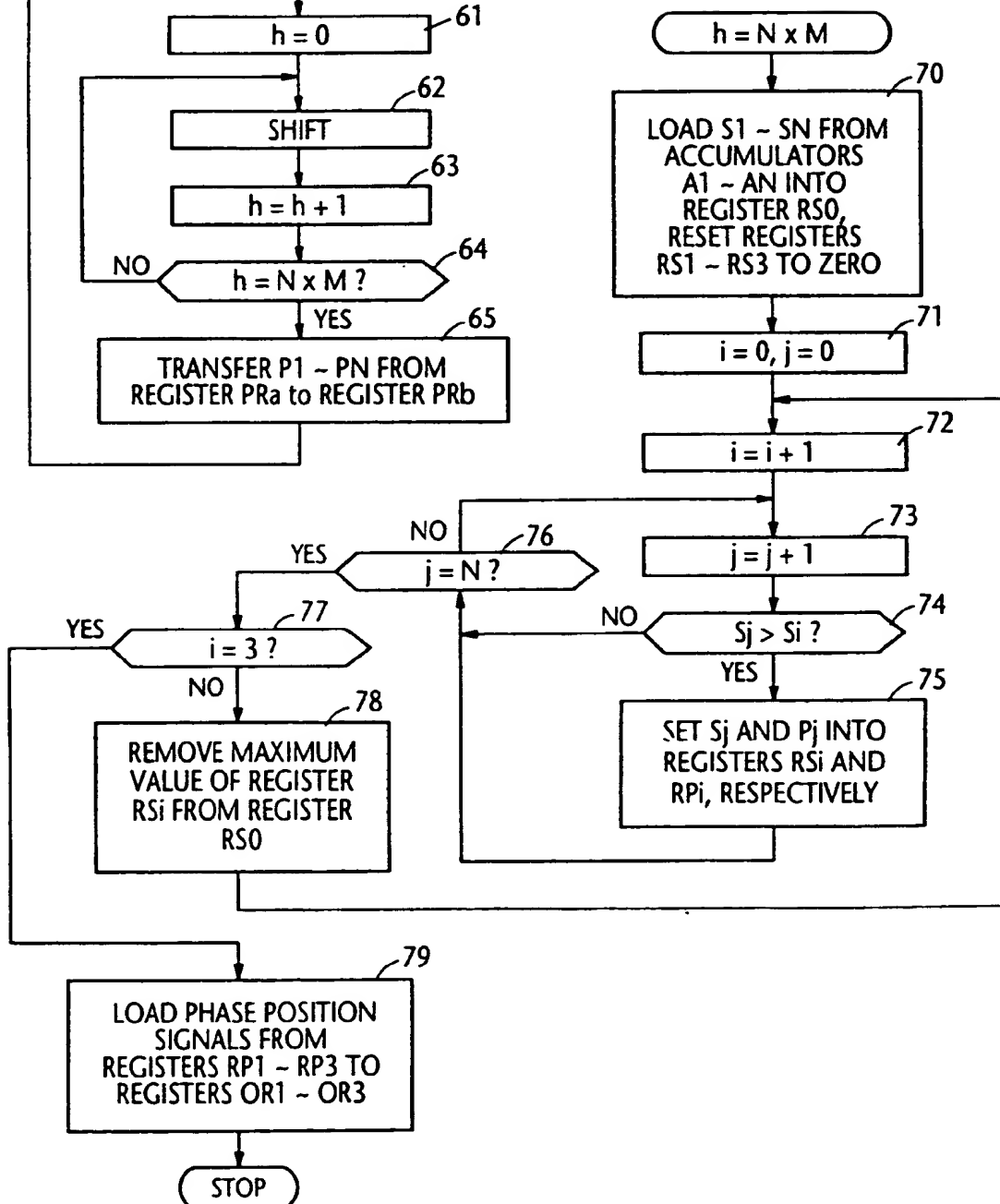


FIG. 4**FIG. 5**

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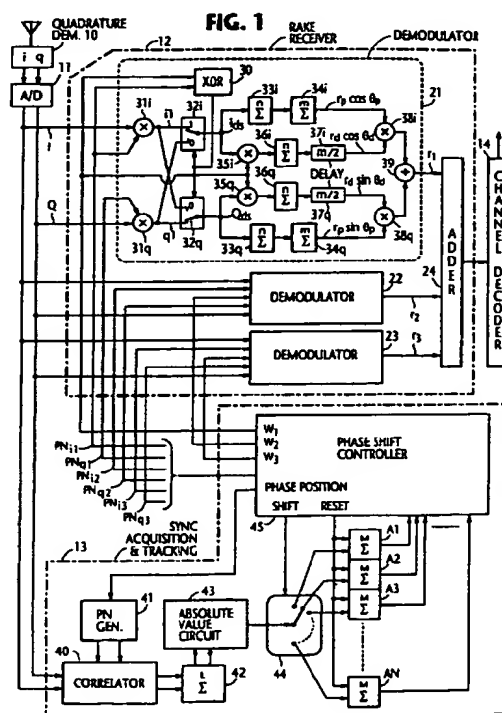
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(54) **Direct sequence spread spectrum receiver using pilot signal averaged over a fixed moving time interval**

(57) In a direct sequence spread spectrum receiver, spread orthogonal data signals and spread orthogonal pilot signals are correlated with orthogonal despreading sequences at a chip rate. These despread signals are integrated at a symbol rate to produce orthogonal data symbols and orthogonal pilot symbols. A predetermined number of pilot symbols of each phase component is moving-averaged. Each phase component of the orthogonal data symbols is weighted with the moving average value of the corresponding phase component of the pilot symbols, and summed with the other weighted component of the data symbols to produce an output signal of the spread spectrum receiver.



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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO 91 07036 A (QUALCOMM INC) * abstract * * page 18, line 22 - line 35 * * page 19, line 1 - line 32 * * claims 1-3; figures 2,3 *	1-4,7-10	H04B1/707
A	US 4 901 307 A (GILHOUSEN KLEIN S ET AL) * column 24, line 66 - line 68 * * column 27, line 24 - line 68 * * column 28, line 1 - line 68 * * column 29, line 1 - line 8 * * figure 15 *	1-4,7-10	
A	GROB U ET AL: "MICROCELLULAR DIRECT-SEQUENCE SPREAD-SPECTRUM RADIO SYSTEM USING N-PATH RAKE RECEIVER" IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, vol. 8, no. 5, 1 June 1990, pages 772-780, XP000175420 * abstract; figure 8 *	1-4,7-10	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H04B
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 3 February 1998	Examiner Harris, E
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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